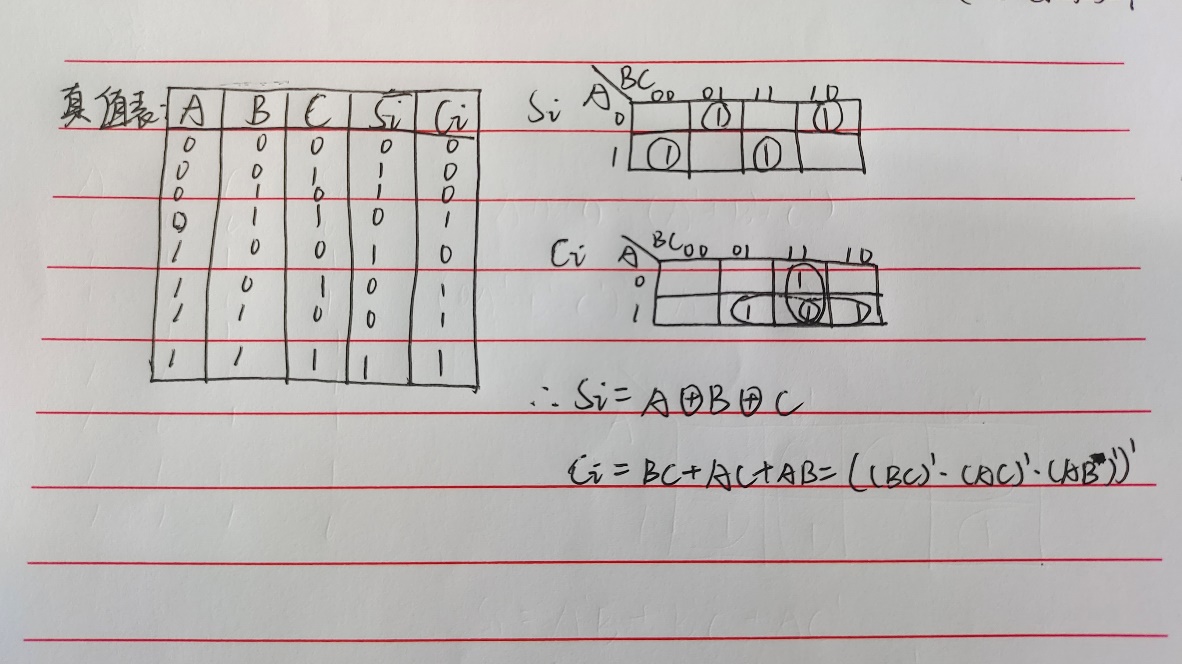
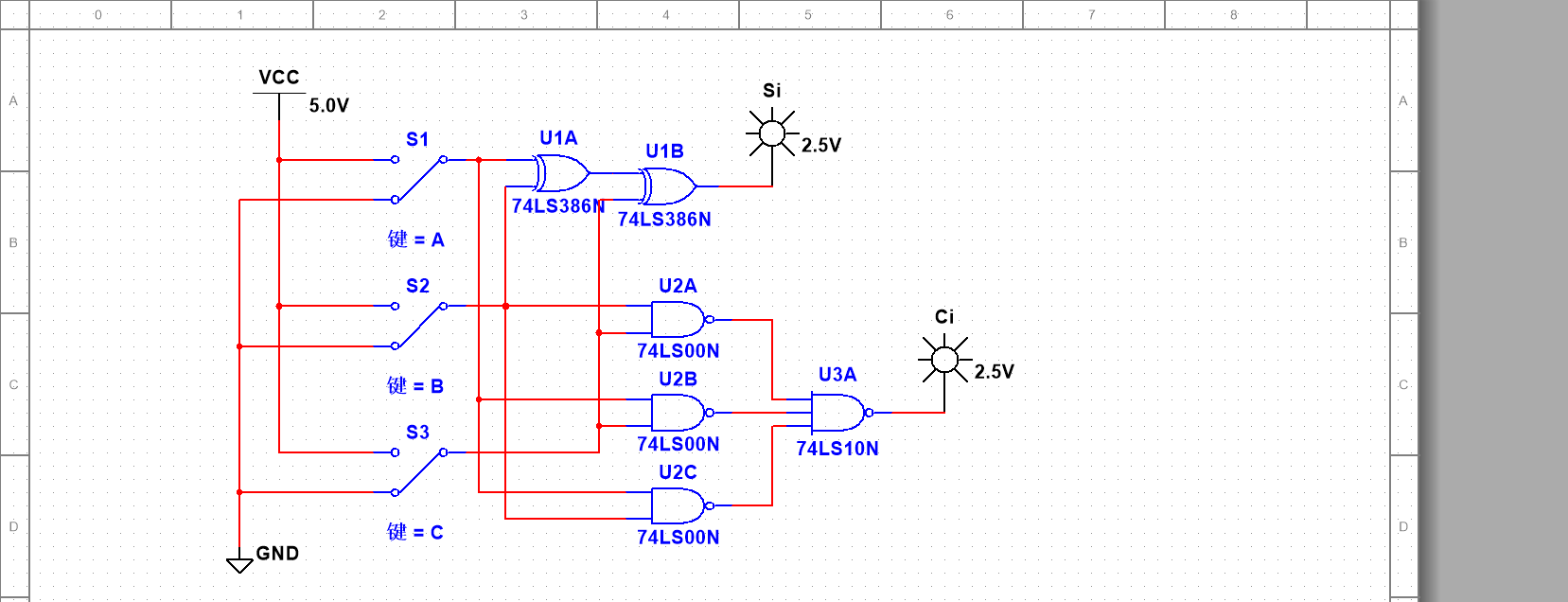
**实验一 实验报告**

1. **全加器**

纸质表、卡诺图化简及逻辑表达式：

****

电路图：

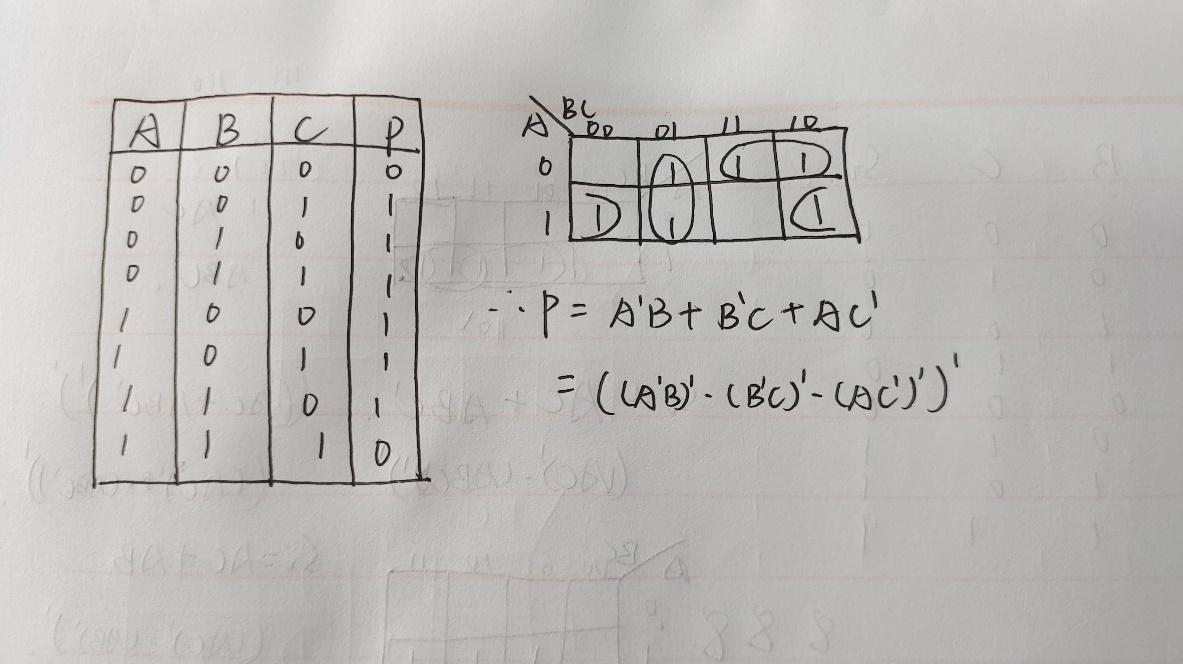


测试结果：

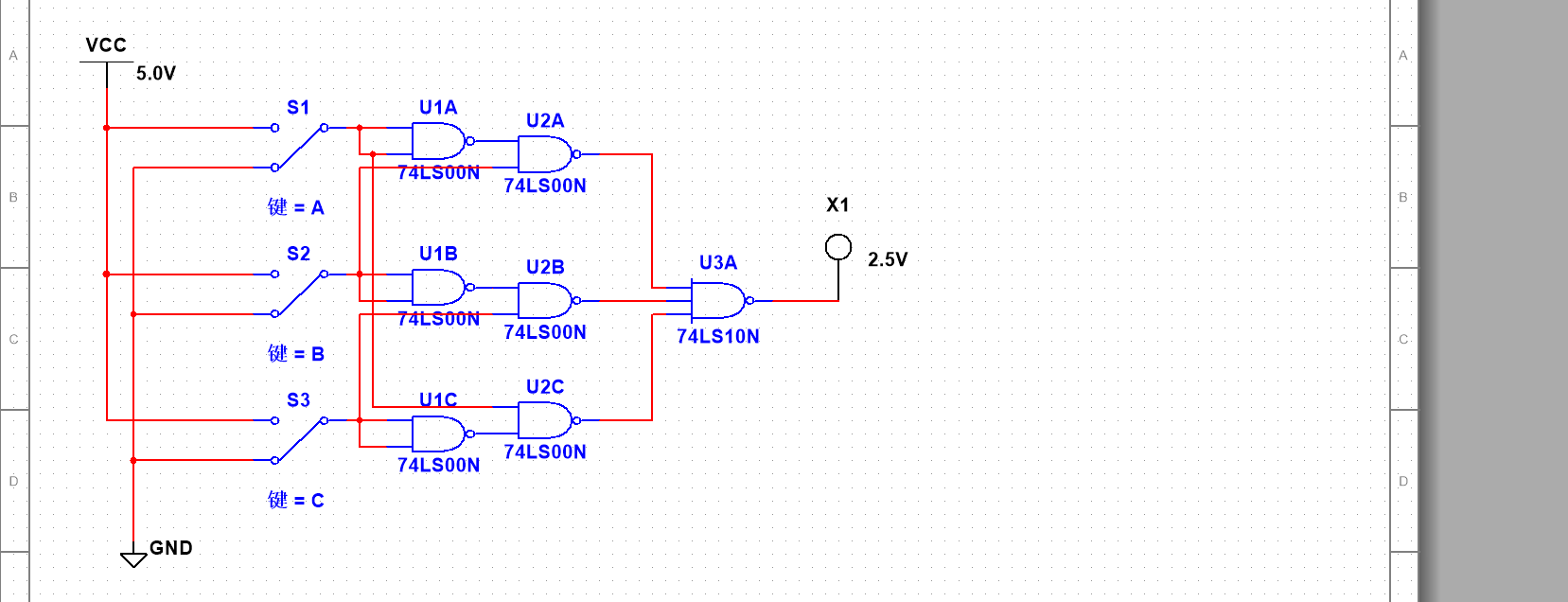
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Ai | Bi | Ci-1 | Si | Ci |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

1. **三变量不一致电路**

纸质表、卡诺图化简及逻辑表达式：



电路图：

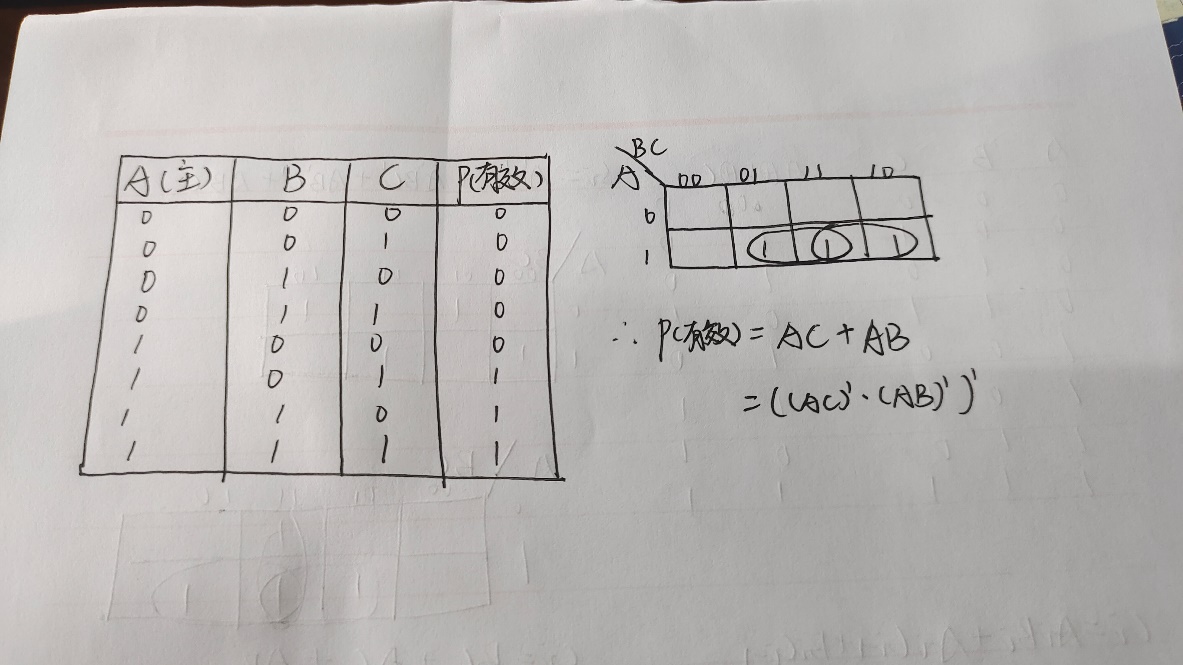


测试结果：

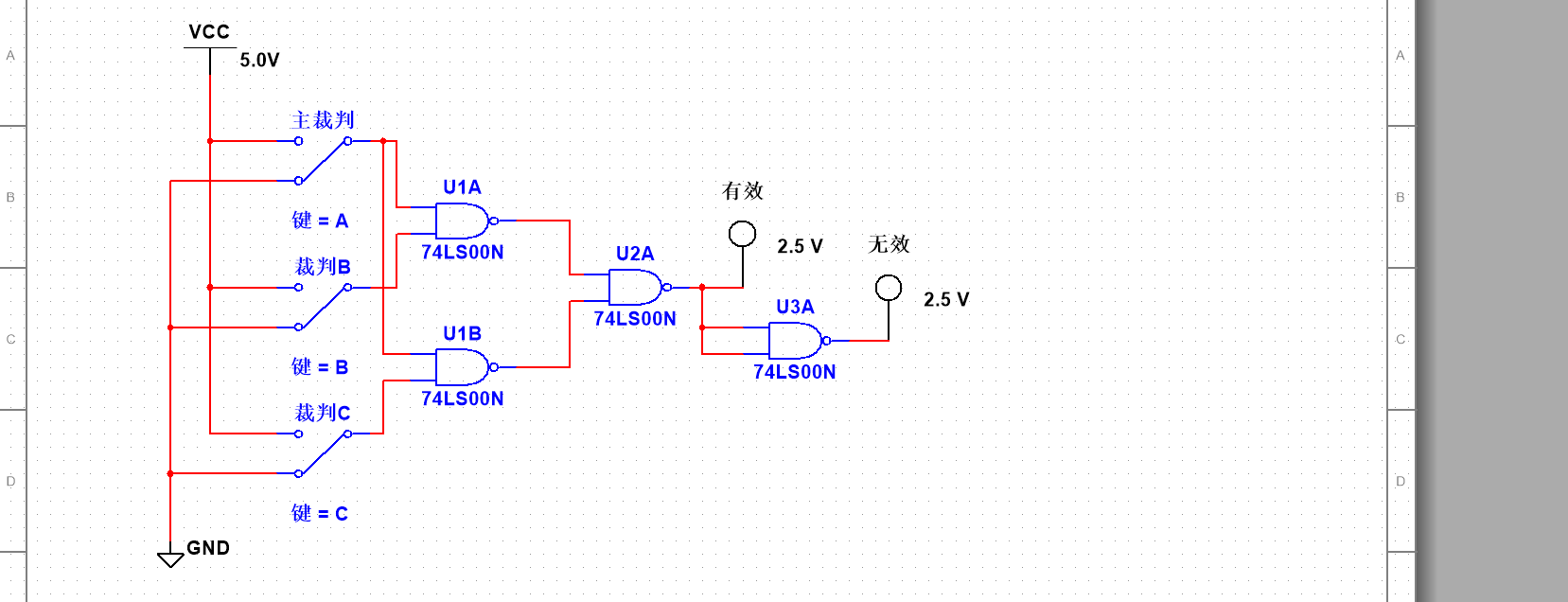
|  |  |  |  |
| --- | --- | --- | --- |
| Ai | Bi | Ci | P |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

**（三）裁判表决电路**

纸质表、卡诺图化简及逻辑表达式:



电路图：



测试结果：

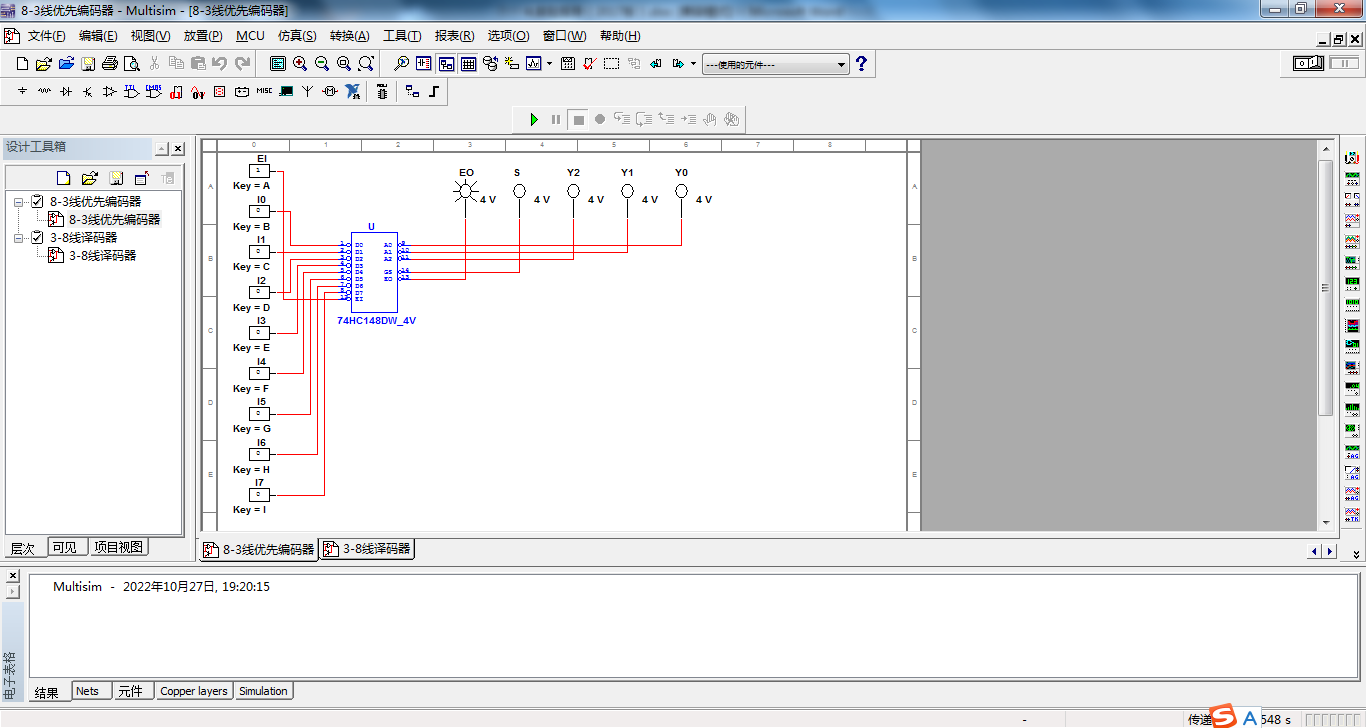
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 裁判A(主) | 裁判B | 裁判C | P（有效） | Q（无效） |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 |

**（四）简易自动售票机**

**实验二 实验报告**

**（一）8-3线优先编码器的测试**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| EI | I0 | I1 | I2 | I3 | I4 | I5 | I6 | I7 | Y2 | Y1 | Y0 | S | E0 |
| 1 | × | × | × | × | × | × | × | × | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | × | × | × | × | × | × | × | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | × | × | × | × | × | × | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | × | × | × | × | × | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | × | × | × | × | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | × | × | × | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | × | × | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | × | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |



**从真值表可以看出：**

**EI只有是低电平的时候，该芯片才工作；**

**I7看做是最低位，I0看做最高位；**

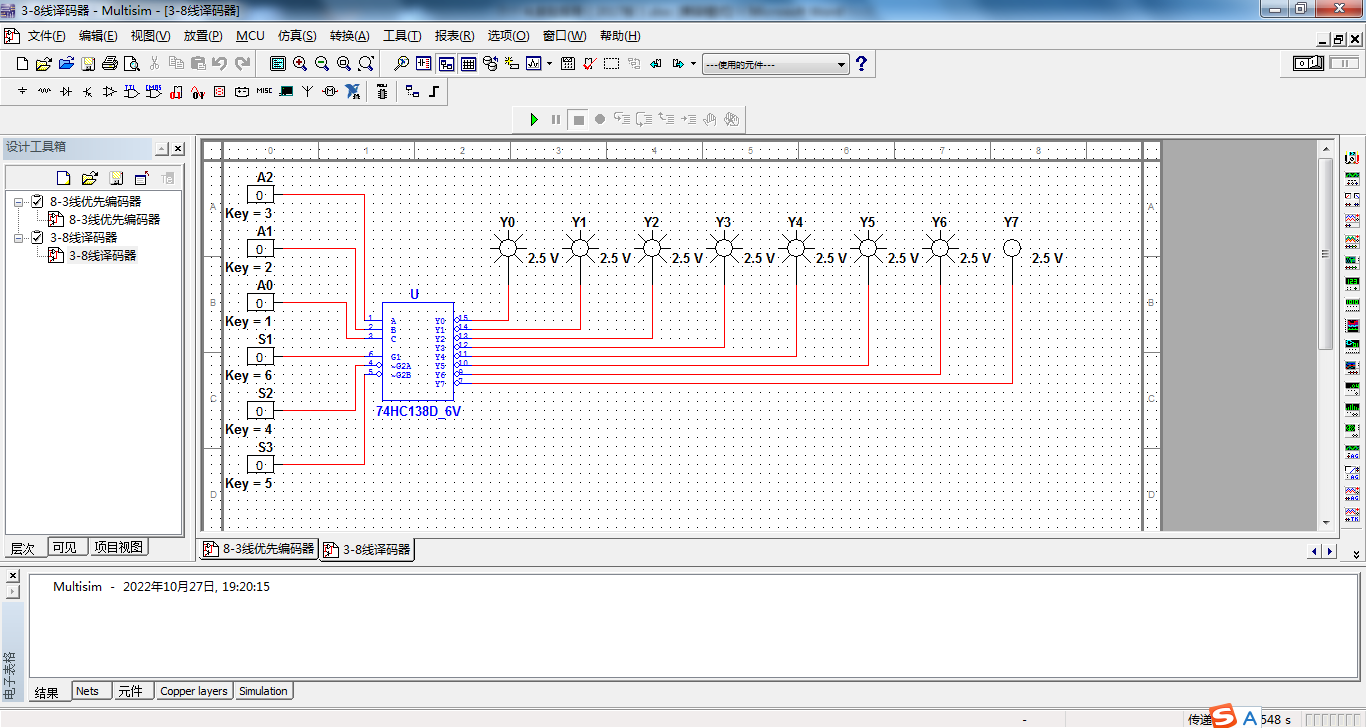
**Y2，Y1，Y0遵循8421码的规律；**

**只要有输入，GS就输出低电平；**

**I7的优先级最高，I0的优先级最低，且低电平为有效输入；**

**（二）3-8线译码器的测试**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 使 能 | | 选 择 | | | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| S1 | S2+S3 | A2 | A1 | A0 |
| × | 1 | × | × | × | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | × | × | × | × | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| l | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |



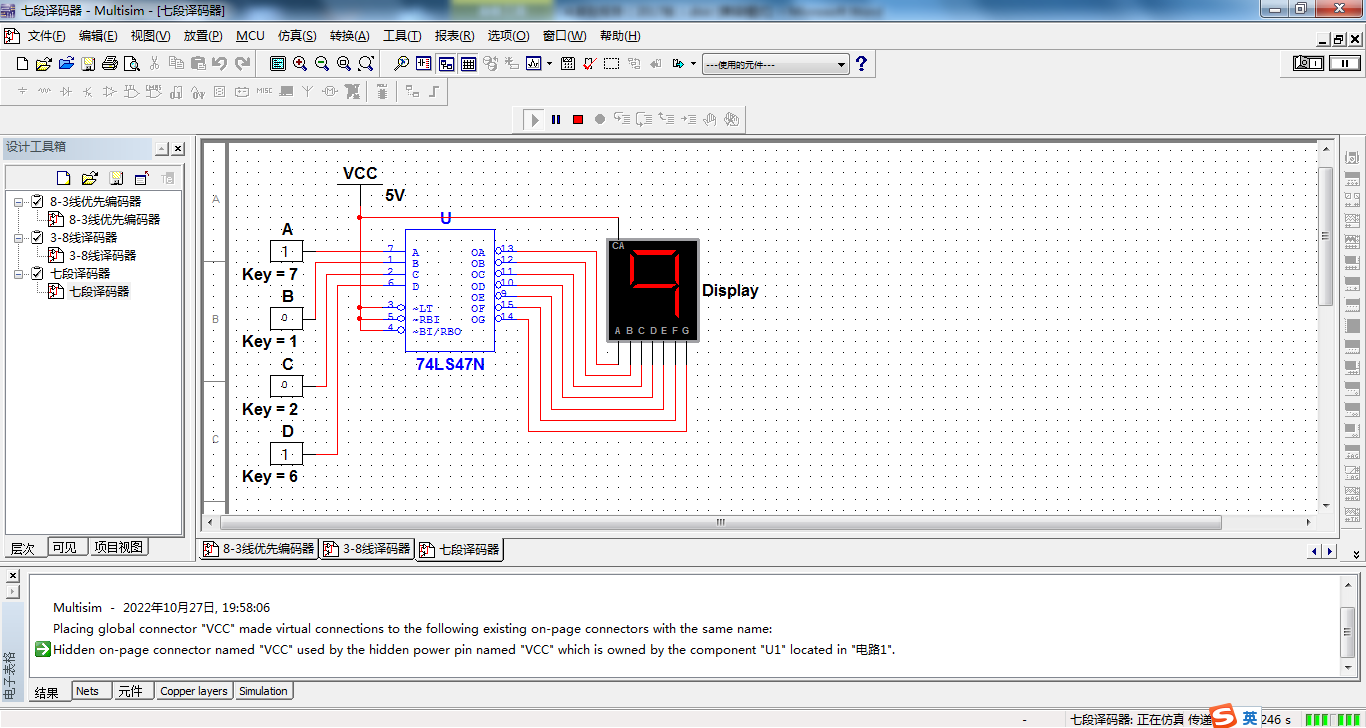
**从真值表可以看出：**

**当S1为0或者S2+S3为1时所有输出端都被封锁在高电平，**

**只有当S1为1和S2+S3为0时，该芯片正常工作。**

**（三）七段译码器的测试**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| D | C | B | A | a | b | c | d | e | f | g |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

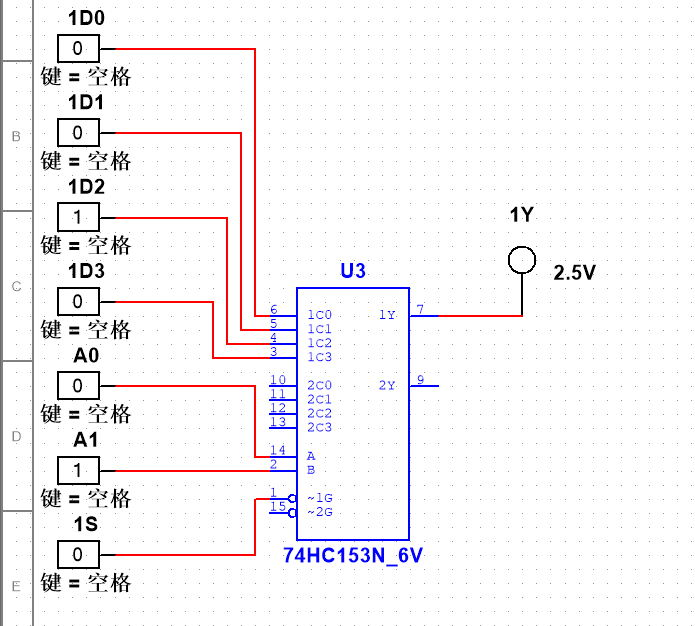


**七段数码管的CA接了一个VCC电源，使用了公共阳极，所以数码管予以显示的位置反而是低电平，用0表示。**

**（四）4选1数据选择器**

1. 4选1数据选择器的测试

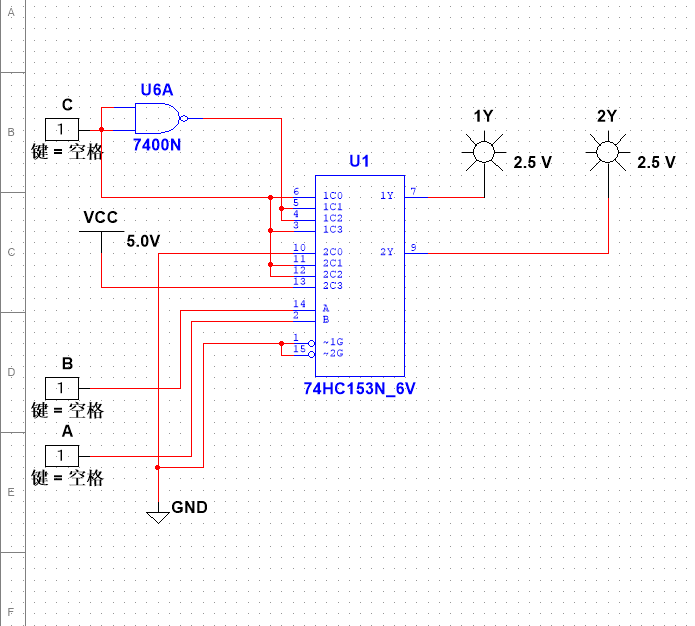
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| lS | A1 | A0 | 1D3 | 1D2 | 1D1 | 1D0 | 1Y |
| 1 | × | × | × | × | × | × | 0 |
| 0 | 0 | 0 | × | × | × | 0 | 0 |
| 1 | 1 |
| 0 | 0 | 1 | × | × | 0 | × | 0 |
| 1 | 1 |
| 0 | 1 | 0 | × | 0 | × | × | 0 |
| 1 | 1 |
| 0 | 1 | 1 | 0 | × | × | × | 0 |
| 1 | 1 |



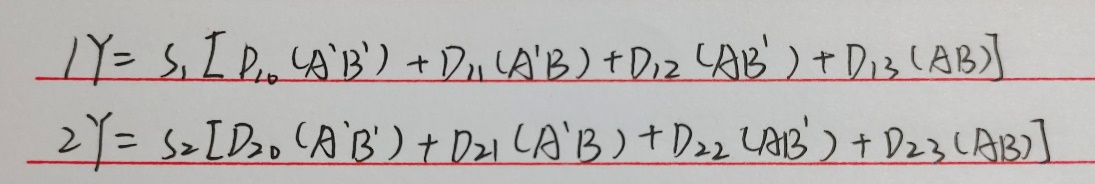
**当S1=1时，不会工作，当S1=0时开始工作。**

2. 4选1数据选择器的分析

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | 1Y | 2Y |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |



根据测试结果的数据分析，可得到输出函数1Y和2Y的逻辑表达式为：



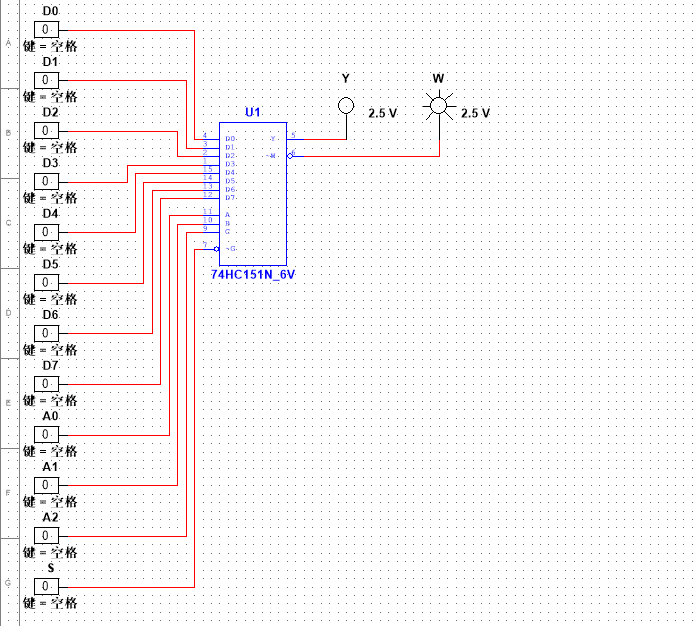
该电路的逻辑功能为：

**从多路数据中选择其中一路信号发送出去，是一个多输入、单输出的组合逻辑电路。**

**（五）8选1数据选择器**

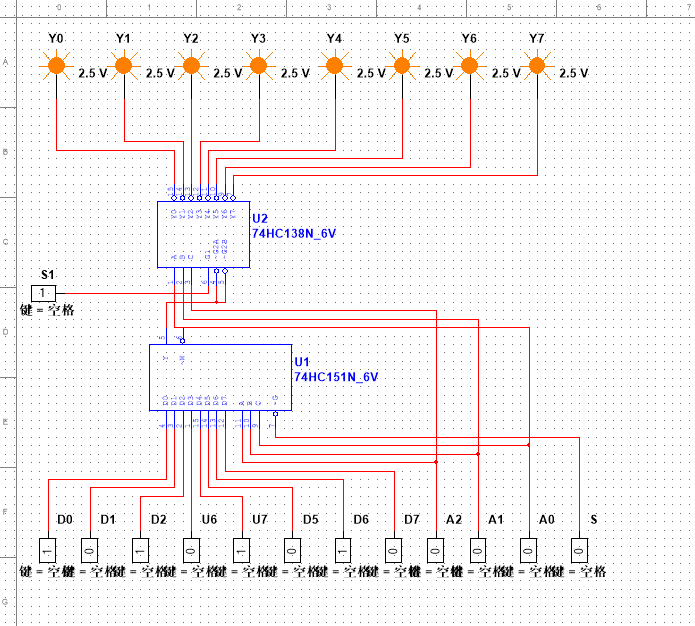
1. 8选1数据选择器的测试

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| S | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Y | W |
| 1 | × | × | × | × | × | × | × | × | × | × | × | 0 | 1 |
| 0 | 0 | 0 | 0 | × | × | × | × | × | × | × | 0 | 0 | 1 |
| 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | × | × | × | × | × | × | 0 | × | 0 | 1 |
| 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | × | × | × | × | × | 0 | × | × | 0 | 1 |
| 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | × | × | × | × | 0 | × | × | × | 0 | 1 |
| 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | × | × | × | 0 | × | × | × | × | 0 | 1 |
| 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | × | × | 0 | × | × | × | × | × | 0 | 1 |
| 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | × | 0 | × | × | × | × | × | × | 0 | 1 |
| 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | × | × | × | × | × | × | × | 0 | 1 |
| 1 | 1 | 0 |



2. 8选1数据选择器的分析

|  |  |  |
| --- | --- | --- |
| D0 D1 D2 D3 D4 D5 D6 D7 | A2 A1 A0 | L0 L1 L2 L3 L4 L5 L6 L7 |
| 1111 0000 | 0 0 0 | 1 1 1 1 1 1 1 1 |
| 0 0 1 | 1 0 1 1 1 1 1 1 |
| 0 1 0 | 1 1 1 1 1 1 1 1 |
| 0 1 1 | 1 1 1 0 1 1 1 1 |
| 1 0 0 | 1 1 1 1 1 1 1 1 |
| 1 0 1 | 1 1 1 1 1 0 1 1 |
| 1 1 0 | 1 1 1 1 1 1 1 1 |
| 1 1 1 | 1 1 1 1 1 1 1 0 |
| 1010 1010 | 0 0 0 | 1 1 1 1 1 1 1 1 |
| 0 0 1 | 1 1 1 1 1 1 1 1 |
| 0 1 0 | 1 1 1 1 1 1 1 1 |
| 0 1 1 | 1 1 1 1 1 1 1 1 |
| 1 0 0 | 1 1 1 1 0 1 1 1 |
| 1 0 1 | 1 1 1 1 1 0 1 1 |
| 1 1 0 | 1 1 1 1 1 1 0 1 |
| 1 1 1 | 1 1 1 1 1 1 1 0 |



根据对测试结果的分析，该电路所完成的功能是：

**从可以根据需要从8路数据传送中选出一路电路进行信号切换，是一个多输入、单输出的组合逻辑电路。**

**实验三 实验报告**

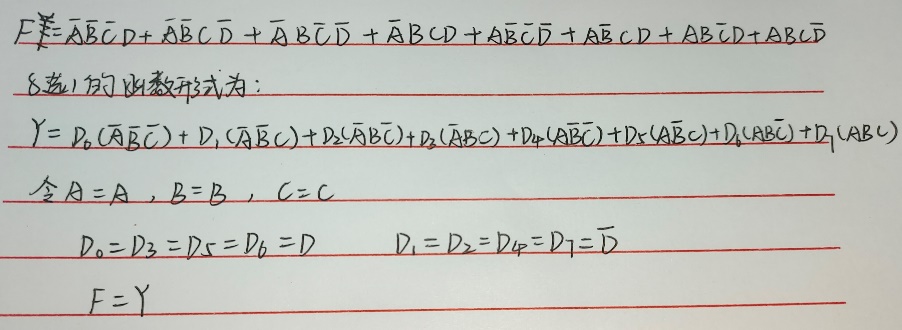
**（一）路灯控制电路**

画出所设计的逻辑电路图，并作简要说明。

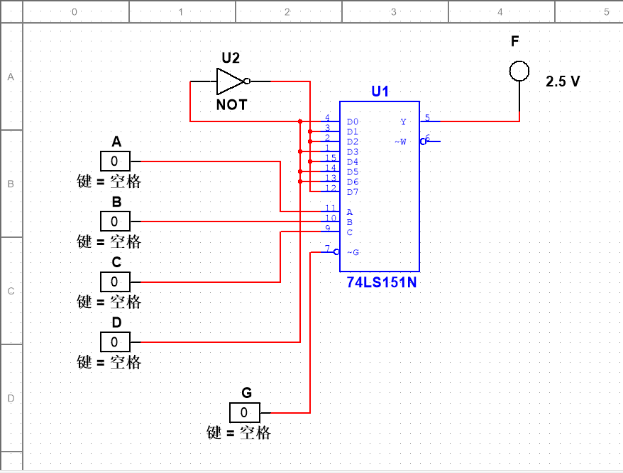
真值表：

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | D | F |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 |

表达式：



电路图：



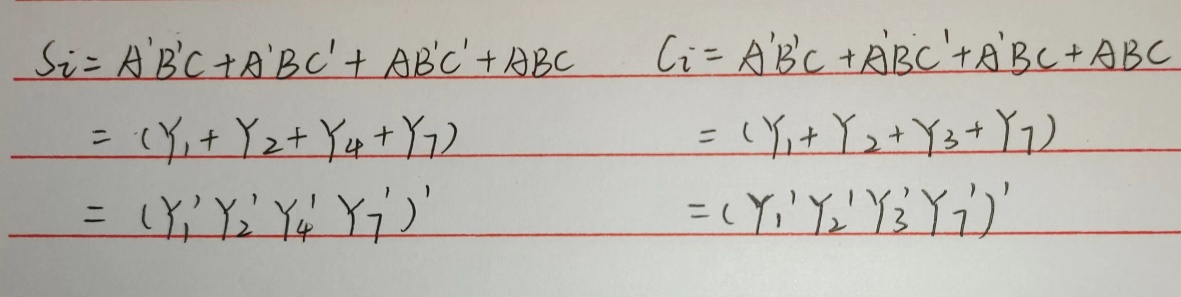
**（二）译码器设计的一位全减器**

画出所设计的逻辑电路图，并作简要说明。

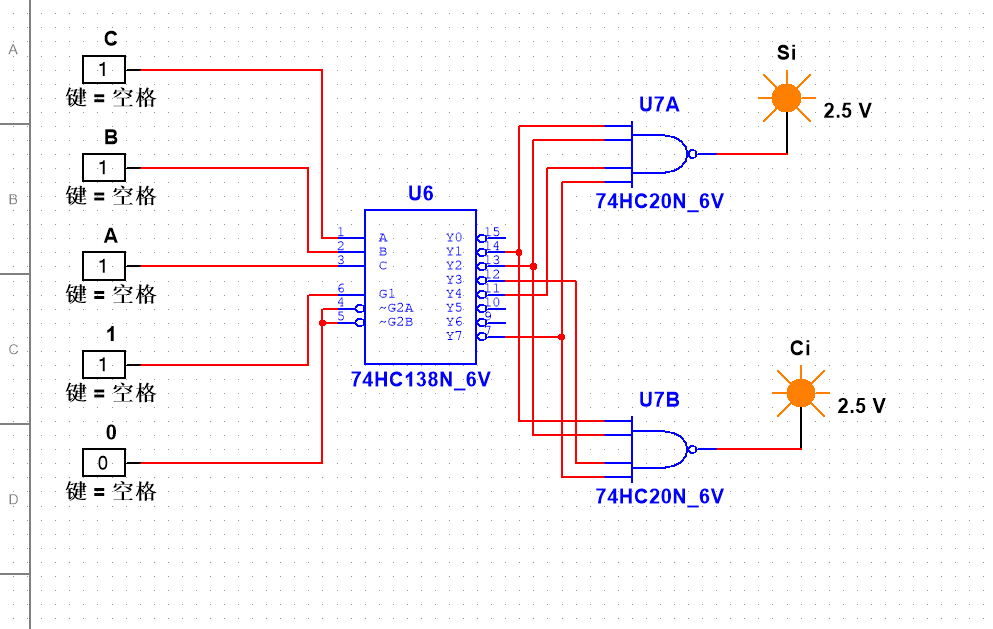
真值表：

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Ai | Bi | Ci-1 | Si | Ci |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

表达式：



电路图：



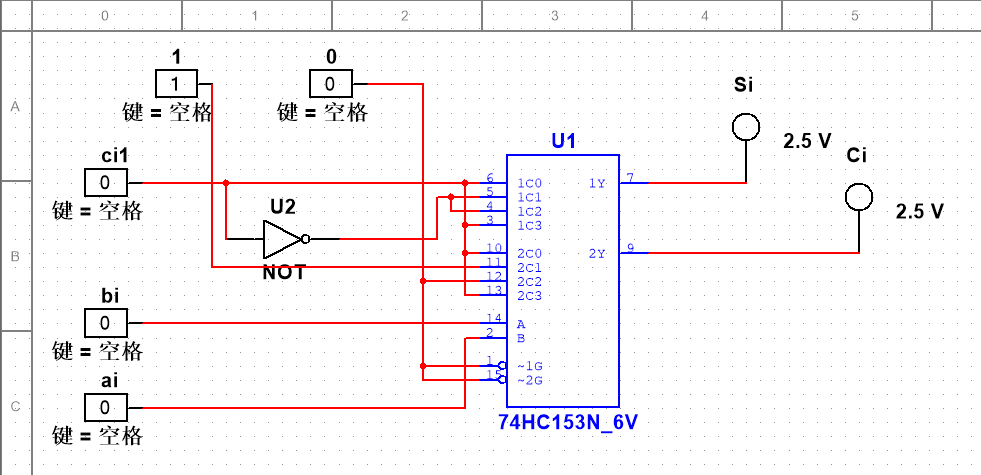
**（三）数据选择器设计的一位全减器**

画出所设计的逻辑电路图，并作简要说明。

真值表：

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Ai | Bi | Ci-1 | Si | Ci |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

电路图：



**实验四 实验报告**

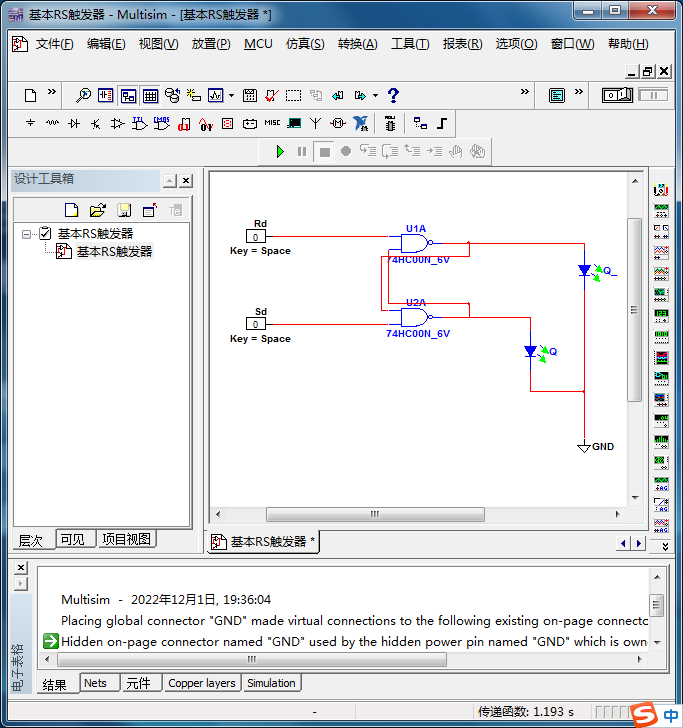
**（一）基本RS触发器**

|  |  |  |  |
| --- | --- | --- | --- |
| Rd | Sd | Q |  |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 |

基本RS触发器的功能是：置位、复位和保持（记忆）功能

它的触发方式是：电平触发，低电平有效

电路图:



**（二）D触发器**

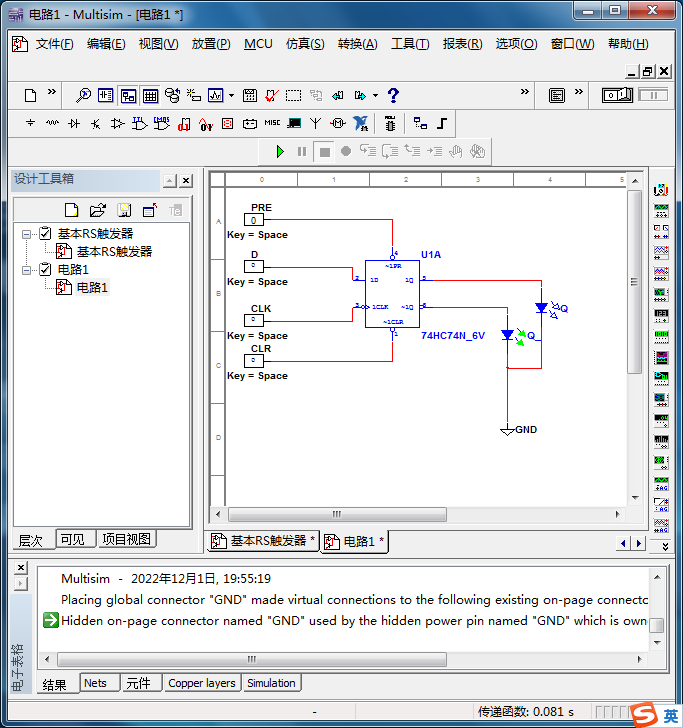
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| CLK | D | PRE | CLR | Q |  |
| 0 | × | 0 | 1 | 1 | 0 |
| 0 | × | 1 | 0 | 0 | 1 |
| 1 | × | 0 | 1 | 1 | 0 |
| 1 | × | 1 | 0 | 0 | 1 |

|  |  |  |  |
| --- | --- | --- | --- |
| D | CLK | Qn+1 | |
| Qn=0 | Qn=1 |
| 0 | ↑ | 1 | 0 |
| ↓ | 1 | 0 |
| 1 | ↑ | 1 | 1 |
| ↓ | 0 | 1 |

D触发器的逻辑功能是：置0、置1

它的触发方式是：电平触发和边沿触发

电路图：



**（三）JK触发器**

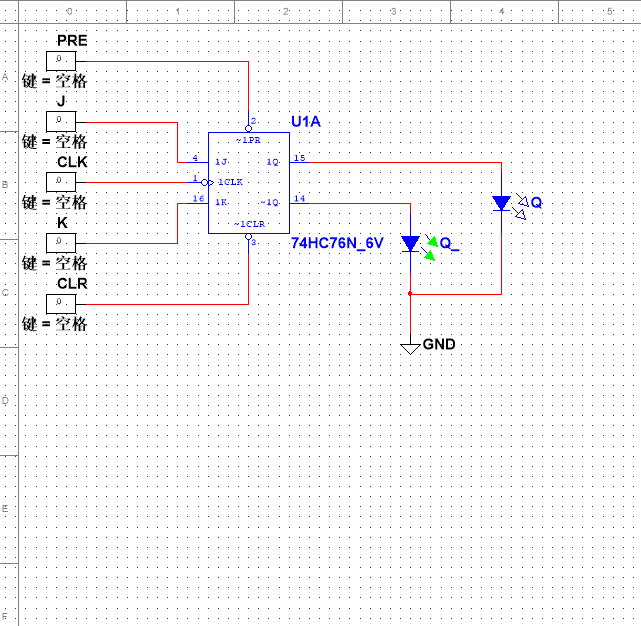
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| CLK | J | K | PRE | CLR | Q |  |
| 0 | × | × | 0 | 1 | 1 | 0 |
| 0 | × | × | 1 | 0 | 0 | 1 |
| 1 | × | × | 0 | 1 | 1 | 0 |
| 1 | × | × | 1 | 0 | 0 | 1 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| J | K | CLK | Qn+1 | |
| Qn=0 | Qn=1 |
| 0 | 0 | ↑ | 1 | 0 |
| ↓ | 1 | 0 |
| 0 | 1 | ↑ | 1 | 0 |
| ↓ | 1 | 0 |
| 1 | 0 | ↑ | 1 | 0 |
| ↓ | 1 | 1 |
| 1 | 1 | ↑ | 0 | 1 |
| ↓ | 1 | 1 |

JK触发器的逻辑功能是：置位、复位、保持和计数功能

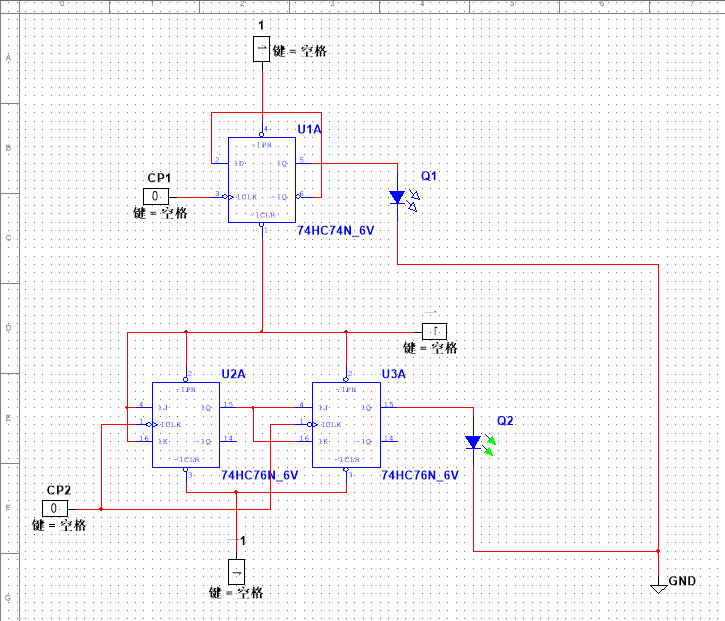
它的触发方式是：边沿触发和电平触发

电路图：

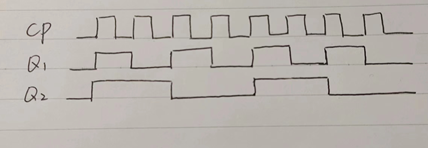


**（四）触发器的应用**

|  |  |  |  |
| --- | --- | --- | --- |
| CP | | Q1 | Q2 |
| 0 |  | 0 | 0 |
| 1 | ↑ | 1 | 0 |
| ↓ | 0 | 1 |
| 2 | ↑ | 1 | 0 |
| ↓ | 0 | 0 |
| 3 | ↑ | 1 | 0 |
| ↓ | 0 | 1 |
| 4 | ↑ | 1 | 0 |
| ↓ | 0 | 0 |
| 5 | ↑ | 1 | 0 |
| ↓ | 0 | 1 |
| 6 | ↑ | 1 | 0 |
| ↓ | 0 | 0 |
| 7 | ↑ | 1 | 0 |
| ↓ | 0 | 1 |
| 8 | ↑ | 1 | 0 |
| ↓ | 0 | 0 |
| 9 | ↑ | 1 | 0 |
| ↓ | 0 | 1 |



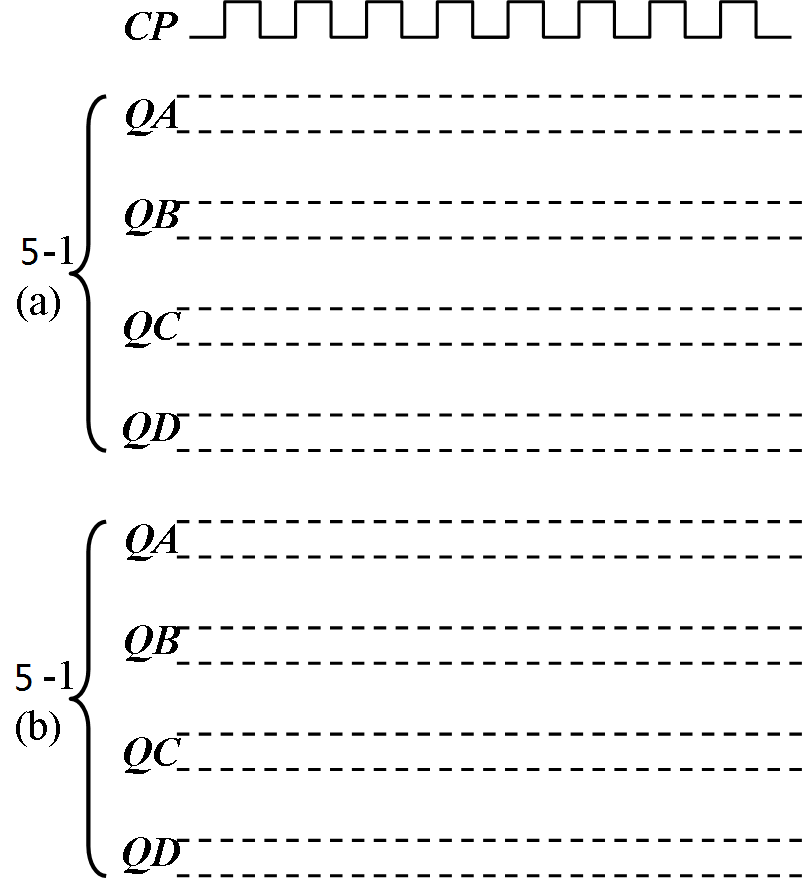
Q1和Q2的波形是：

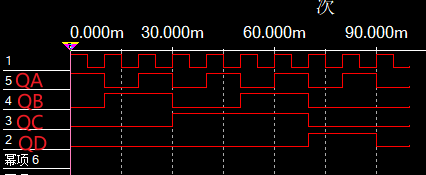


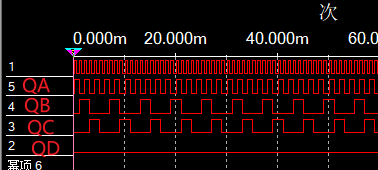
### 实验五 实验报告

**（一）同步十进制计数器**

1. 画出图5-1(a)和5-1(b)中电路输出信号的波形：



５－１（ａ）

５－１（ｂ）

2.

图5-2中计数器的进制是：百进制

它的工作原理是：

用两个十进制计数器，把其中一个十进制计数器的进位输出端接到另一个十进制计数器的时钟信号端。

当第一个十进制计数器从9变0时，它的进位输出端从低电平变高电平，从而导致第二个十进制计数器的时钟信号端产生一个下降沿，使第二个十进制计数器完成了一次计数。

最终组合实现了两位的计数器，实现了从00——99的百进制计数器。

**（二）双向移位寄存器**

1.

图5-3中74HC194的作用过程是：

表5-3a：

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| CP | 输入D | S1 | S0 | QA | QB | QC | QD |
| 0 | 1011 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1011 | 1 | 1 | 1 | 1 | 0 | 1 |

表5-3b：

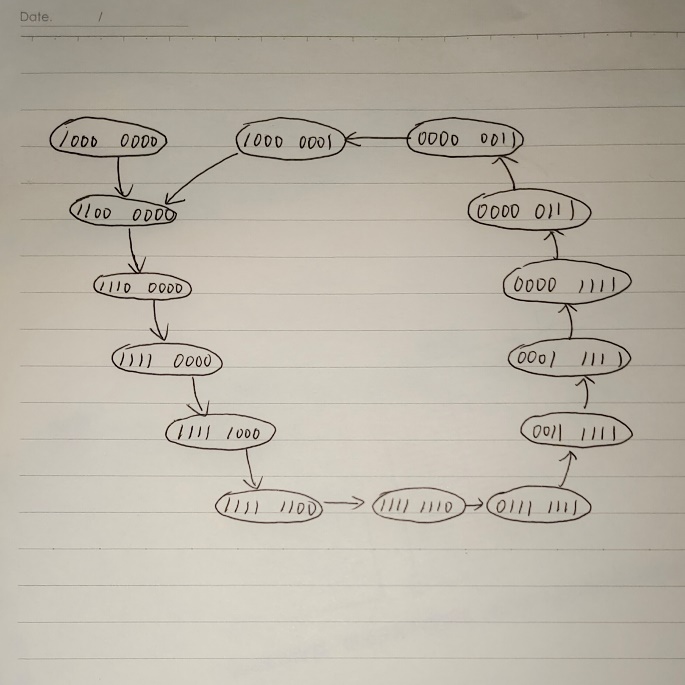
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| CP | 输入D | S1 | S0 | QA | QB | QC | QD |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 2 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 3 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 4 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |

表5-3c：

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| CP | 输入D | S1 | S0 | QA | QB | QC | QD |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 3 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 4 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |

2. 图5-4中的计数器所完成的功能：13进制计数器；

状态转移图：

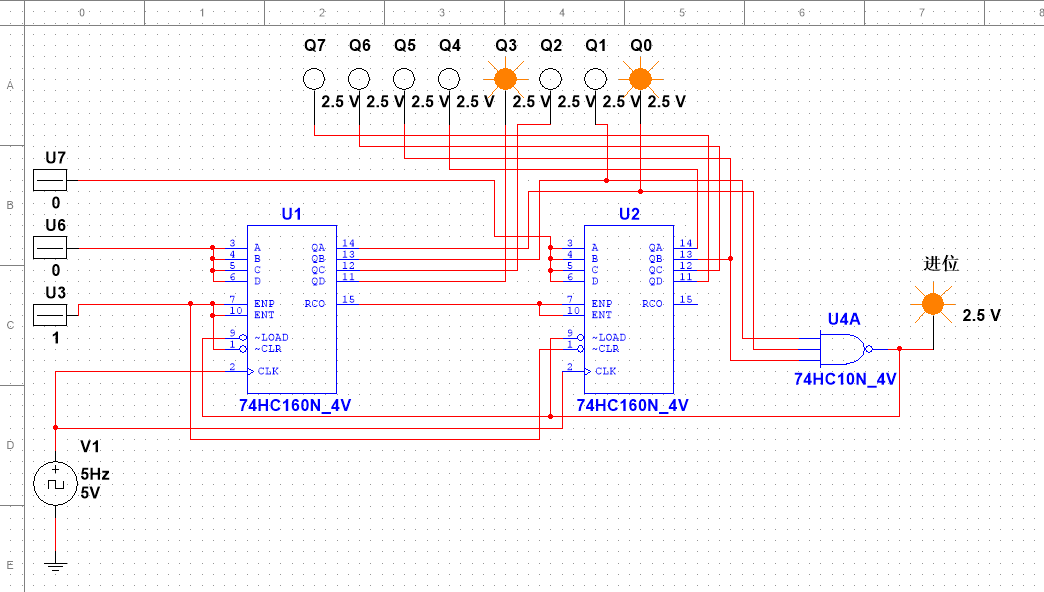


### 实验六 实验报告

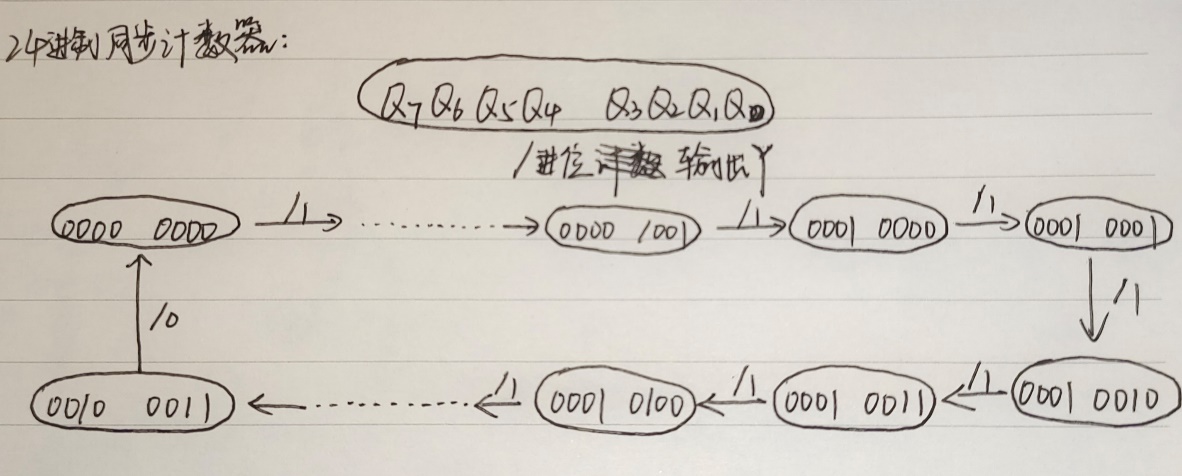
**1. 24进制同步计数器电路图：**

设计思路：74HC160为同步十进制计数器芯片，即N（10进制）<M（24进制），可以利用整体置数法。利用并行进位法将两片74HC160接成N’（100进制）>M（24进制）的计数器，之后再通过置数法接成24进制同步计数器。

电路图：



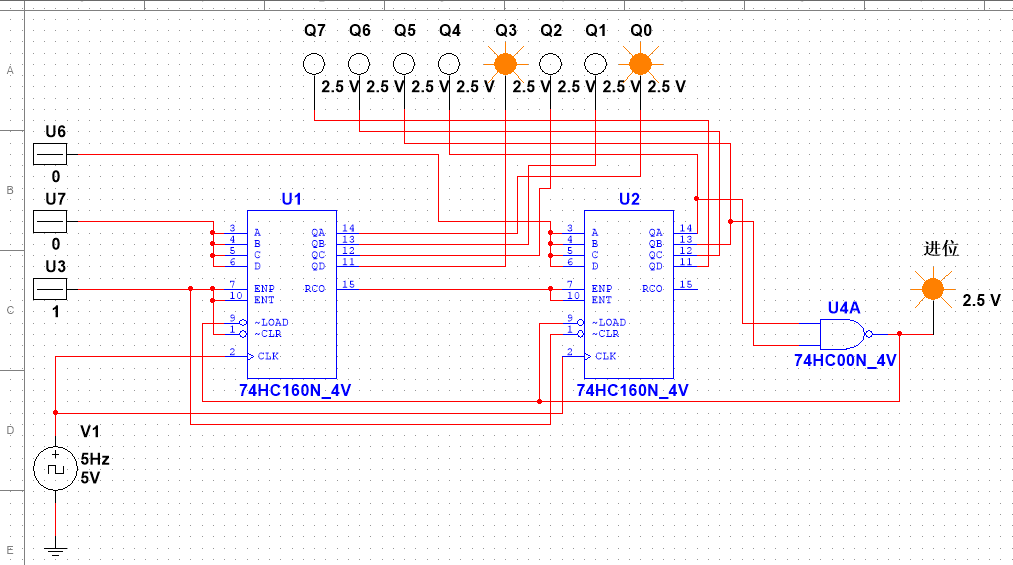
状态转换图：



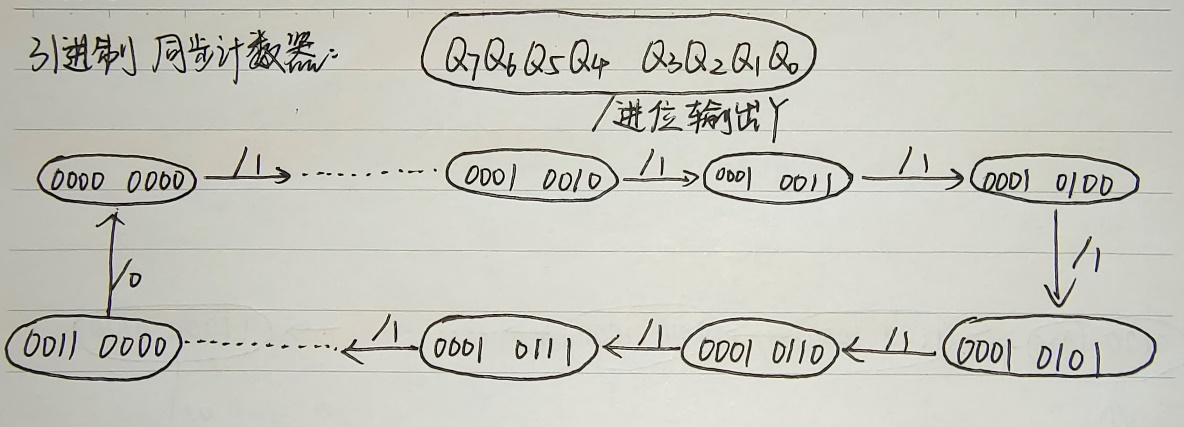
**2. 31进制同步计数器电路图：**

设计思路： 74HC160为同步十进制计数器芯片，即N（10进制）<M（31进制），可以采用整体置数法。利用并行进位法将两片74HC160接成N’（100进制）>M（31进制）的计数器，之后再通过置数法接成31进制同步计数器。

电路图：



状态转换图：



**3. 模13扭环计数器电路图：**

设计思路：模13扭环计数器即为用74HC194设计出的13进制的计数器，要使用两个74HCl94移位寄存器，可以做到16（2\*8）进制计数器，由于其工作状态保持右移，则可将最后一位舍弃，即只用7位来设计出14（2\*7）进制的计数器。最后，只需要把第6、7位的输出做与非门共同构成反馈线作为移入数据，则可将‘0000000’的输出信号舍弃，达到模13扭环计数器。

电路图：

